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Fan Li, Ang Li, Shiqiang Wu, Weisheng Wang, Yuhao Zhu, Wen Liu*, GuoHao Yu*, Zhongming Zeng, Baoshun Zhang

***Abstract*— This article presents the monolithic integrated circuit (IC) platform based on the hydrogen plasma treated (H-treated) p-GaN HEMTs technology that realizes point-of-load 48 V - 1 V DC-DC power conversion. The direct-coupled FET logic (DCFL) circuit and driver module are successfully implemented. The power device, diode, capacitor and resistors are integrated on the same platform. In addition, accurate modeling of the Enhancement and Depletion (E/D-) mode devices in circuit modules is facilitated using the ASM-HEMT model. The device characteristics are extracted to calibrate the model parameters for the computer-aided circuit design. Excellent agreement between simulation and experimental results for static and dynamic circuit performance is verified through inverter and comparator circuits. This approach ensures the development of a GaN DC-DC power converter system, including a gate driver module and a power device that operates at 1 MHz. The work paves the way for scaling up the monolithic GaN mixed-signal power IC.**

***Index Terms*— GaN HEMT, Integrated Circuits, Hydrogen Passivation, ASM Simulation, DC-DC Converter.**

I. Introduction

The use of Gallium Nitride (GaN) in power electronics has seen an enormous rise due to its remarkable characteristics, such as improved breakdown voltage, high-temperature capabilities, and fast switching speed [1]. In GaN power electronics, a widely adopted Enhancement-mode (E-mode) technique involves utilizing a p-GaN gate structure. However, the commercialization of normally-off p-GaN technology faces a significant challenge, namely the etch damage induced by Cl-based plasma etching, leading to additional reliability issues. To tackle the reliability concerns from surface damage issues in p-GaN gate HEMT, etch-free techniques have been developed using hydrogen plasma treatment (shorted as the H-treated device) [2], yielding optimal electrical outcomes, as demonstrated in prior studies [3].

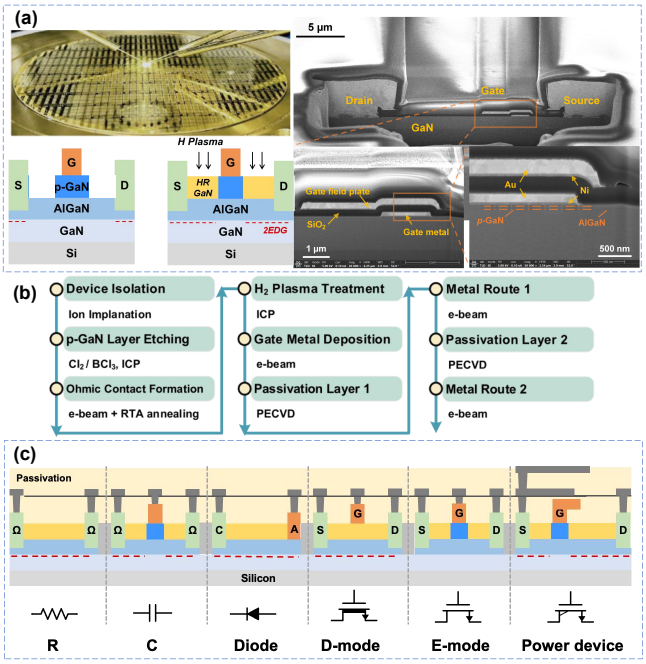

Fig. 1. (a) The etched and H-treated device structure and FIB cross-sectional images of the H-treated power device. (b) The fabrication process of the 4-inch H-treated p-GaN wafer. (c) The demonstration of components within the proposed IC platform.

With the desire to improve the efficiency and power density of GaN-based systems, monolithic GaN HEMT circuit integration has been achieved on different platforms. The stability and cost-effectiveness of the GaN integration roadmap have been verified [4], [5]. Current research has been focused on exploring the capabilities of GaN transistors and circuits across different logic families, transistor technologies and integration approaches. Despite notable progress, computer-aided design is particularly important in improving integration scalability [6], which involves accurate device modeling for circuit simulations. The Advanced Spice Model (ASM) in GaN Hemt characterization has become a major candidate for device modeling and characterization, which draws research and industry interest [7], [8] by effectively capturing GaN device physical phenomena via surface potential-based first-

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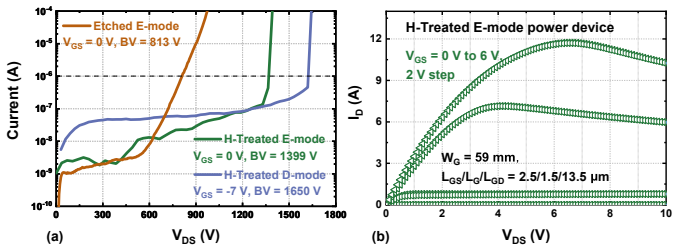

Fig. 2. (a) The OFF-state breakdown characteristics of H-treated E-mode and D-mode devices compared with the etched E-mode device. (b) Output characteristics of H-treated E-mode power device.

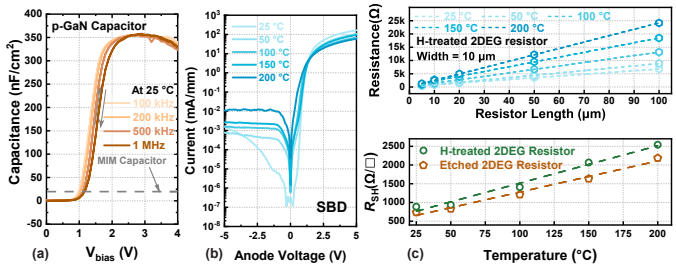

Fig. 3. The circuit components of the (a) capacitor, (b) Schottky barrier diode, and (c) 2DEG resistor and the H-treated IC platform.

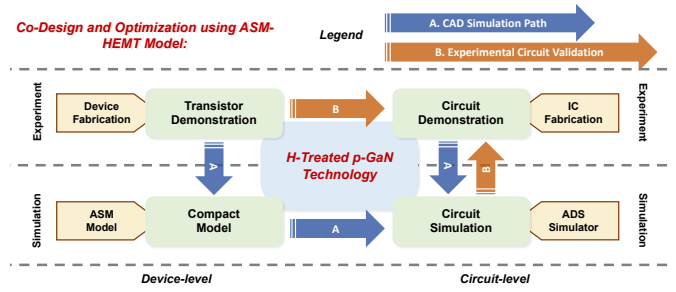

Fig. 4. The roadmap for the computer-aided design and optimization of the proposed IC platform.

principle formulas. This model can be modified and applied for mixed-signal monolithic circuit design and optimization in power electronics.

This study focuses on the design and optimization of the H-treated p-GaN IC power conversion platform using the ASM-HEMT model. The research validates the modeling process via logic blocks and comparator circuits. A monolithic IC has been achieved as a POL 48 V - 1 V GaN DC-DC power converter with a gate driver module and power device.

II. Fabrication and Design Process

Fig. 1 (a) and (b) present the device stricture and fabrication process, and Fig. 1 (c) illustrates the 4-inch GaN HEMTs IC platform achieved in this research and the complete fabrication process. Fig. 2 (a) depicts the breakdown characteristics up to 1399 V of power devices with dimensions of $L_{GS}/L_G/L_{GD}/W_G$ = 3/1.5/13.5/100 μm, demonstrating higher breakdown voltage compared with the etched device. Fig. 2 (b) shows the E-mode power device, featuring a gate width of 59 mm with a maximum output current of 12 A. The other circuit components, including p-GaN and Metal-Insultaor-Metal (MIM) capacitor,

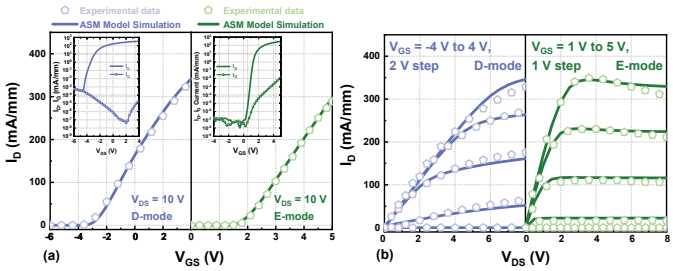

Fig. 5. (a) The transfer and (b) output characteristics of H-treated D/E-mode devices, the solid lines are experimental results, and the dotted lines are the calibrated ASM-HEMT model simulation. inset: transfer characteristics in log scale.

TABLE I
THE KEY DEVICE PARAMETERS OF ASM-GAN HEMTS MODEL

Parameter	E-mode	D-mode	Parameter	Emode	Dmode
nf	3	3	nfactor	0.5	0.5
Vth	1.5	-2.3	cdscd	1e-3	3.8e-1
U0	4.3e-2	3.1e-2	U0accs	6.8e-3	1.7e-3
Ua	3.3	1.2	U0accd	6.8e-3	1.7e-3
Ub	1e-18	2.9e-18	cgso	4e-11	4e-11
eta0	1e-4	0.2	cgdo	1e-14	1e-14
vdscale	1	5	cdso	3e-11	3e-11

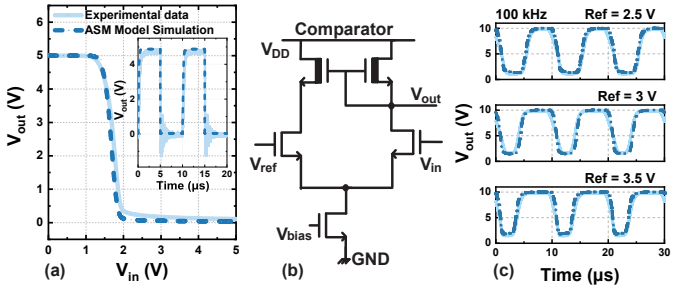

Fig. 6. The experimental results (solid line) and simulation results (dotted line) of (a) The VTC and (b) the dynamic waveform of the DCFL inverter. The (c) demonstrates the comparator structure and (d) shows the agreement between simulation and experimental results.

Schottky barrier diode (SBD) and 2DEG resistors, are also verified on the H-treated IC platform, as shown in the Fig 3.

The computer-aided simulation and circuit design represent a crucial step toward scaling up and eventually design technology co-optimization (DTCO). Fig. 4 presents the workflow for the design and optimization procedure for the monolithic circuit. The calibrated ASM-HEMT model for the H-treated device connects the device and circuit design. Simulating the circuit's static and dynamic performance is crucial in scaling the integrated components. The key design parameters are summarized in Table I. Fig. 5 shows the transfer and output characteristics on the H-treated devices for low-voltage circuit integration with dimensions of $L_{GS}/L_G/L_{GD}$ = 3/1.5/3 μm, showing the alignments between the accurately tuned ASM-HEMT model and the experimental results. The D-mode device utilizes the H-treated p-GaN layer as a dielectric. Fig. 5 (a) presents the transfer curves of the D/E-mode HEMTs. Fig. 5 (b) demonstrates the output curves. An accurate device model calibrated for the H-treated device served as the bridge for the circuit design and assures the feasibility of the IC platform design.

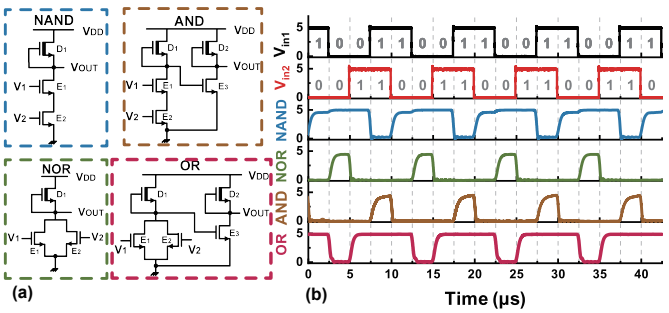

Fig. 7. (a) The schematics of the fabricated logic gates circuit and (b) The dynamic performances of NAND, NOR, AND, and OR logic gates.

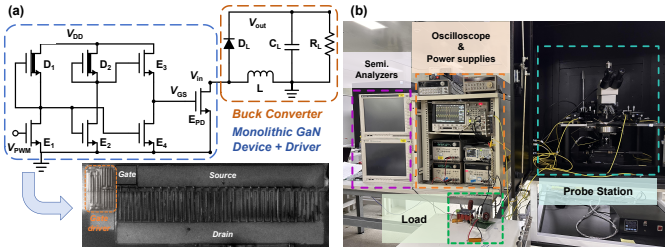

Fig. 8. (a) Circuit diagram of the H-treated p-GaN buck converter with a monolithic integrated gate driver and power device. (b) The photo of the test setup.

III. Performance of the IC Platform Components

The ASM-HEMT model is calibrated to simulate and validate the device/circuit accurately. Fig 6 (a) shows the voltage transfer curve (VTC) of the DCFL inverter, and Fig 6 (b) shows the corresponding output at 160 kHz. The oscillations are due to parasitic inductive effects. Fig 6 (c) and (d) show the output response of the comparator at various reference voltages with a 0.5 V step. Excellent agreement was verified, with minor discrepancies in the rise and fall times for the dynamic characteristics, which may due to the non-idealities of the test setup. Developing mixed-signal ICs achieves a significant milestone by demonstrating logical computational ability. The H-treated device roadmap successfully fabricates logic building blocks, including NAND, NOR, AND, and OR gates, as shown in Fig 7.

The proposed monolithic power converter represents a significant step in advancing hydrogen-treated GaN technologies within power electronics (Fig 8). The buck converter achieves direct DC-DC conversion from 48 V to 1 V at frequencies up to 1 MHz, with C_L = 20 μF, L = 1 mH, R_L = 500 Ω. Fig 9 (a) demonstrates rapid rise and fall timeout of the buffer stage, and the switching characteristics and waveforms exhibit duty cycles ranging from 2% to 98% are exhibited in Fig 9 (b). The output voltage level shows high linearity with the change of the duty cycles, as shown in Fig 9 (c). These results underscore the potential of hydrogen-treated GaN technology, enabling on-chip implementation of GaN power circuits that integrate the driver stage and power device stage for intelligent all-GaN power systems.

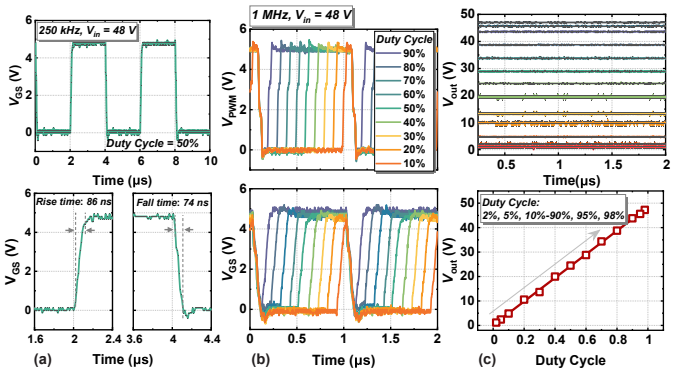

Fig. 9. The bus voltage of converter V_{in} is 48 V. Switching waveforms of (a) driver output V_{GS} and rise/fall time at 250 kHz. (b) Driver input signal V_{PWM} and V_{GS} at 1MHz. (c) Converter output at various duty cycles.

IV. Conclusion

In conclusion, this study advances the H-treated p-GaN HEMTs integration platform. The H-treated device shows improved breakdown voltage. Using the ASM-HEMT model, device characteristics are extracted and calibrated for monolithic circuit simulation, ensuring strong agreement between static characteristics of experimental and simulated circuits. The successful development of a 48 V - 1 V GaN DC-DC power converter operating at 1 MHz represents an achievement in pursuing the full potential of a monolithic GaN power system.

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